UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,024	06/28/2005	Mamiko Akizuki	28951.5400	4042

27890 7590 03/17/2008

STEPTOE & JOHNSON LLP
1330 CONNECTICUT AVENUE, N.W.
WASHINGTON, DC 20036

EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
03/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/541,024	AKIZUKI ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9,10,12-19 and 34-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9, 10, 12-19, 34-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

2. **Claims 15 and 34** are objected to because of the following informalities: in line 4 of both claims the applicant has amended the claims to state "accessing a the memory" the examiner believes the term "the" should have been removed, based on the other claims. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 15, 16 and 19** are rejected under 35 U.S.C. 102(b) as being anticipated by Ochiai et al. (US 6,340,973 B1).

3. Consider **claim 15**, Ochiai et al. discloses a memory controller for controlling a memory having a plurality of banks, **the memory controller**, comprising: an arbitration

circuit for arbitrating a memory access request **from a plurality of blocks** for accessing a memory(Fig. 7, Col. 24 lines 55-67 and Col. 25 lines 1-22); a command generation block for generating a memory command for a memory based on a control signal from the arbitration circuit (Fig. 1, abstract, Col. 5 lines 26-34); an address generation block **for receiving** a memory address from a block permitted **by the arbitration circuit for accessing a memory** and **outputting** the memory address to **such** memory (Fig. 1, abstract, Col. 2 lines 23-25, Col. 5 lines 20-25 and Col. 6 lines 3-7); and a data latch block **for latching either** write data from the block permitted **by the arbitration circuit for accessing a memory** or read data from a memory and passing data between a memory and the block (Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34), bank access data is access data to the memory, comprising a predetermined number of bytes for performing writing or reading on the same bank of the memory, block access data is a data unit comprising two sets of the bank access data belonging to different banks, and the arbitration circuit instructs the command generation block to provide a wait cycle when a memory access request is made by the bank access data alone from the block permitted to access the memory (Fig. 28, Col. 1 lines 31-40 and 65-67, Col. 2 lines 1-2, Col. 5 lines 1-6 and 35-40 and Col. 6 lines 45-51, Col. 7 lines 55-67, Col. 8 lines 1-55 and Col. 12 lines 35-38, where Fig. 28 clearly shows an idle (wait) state after a pre-charge).

4. Consider **claim 16,** as applied to **claim 15** above, Ochiai et al. discloses wherein the arbitration circuit comprises: a request receiving block **for receiving** a memory request from the plurality of blocks, **the request receiving block comprising** a data

unit decision unit for deciding a data unit of requested memory access based on the received memory request, and **providing** an instruction to generate an enabling signal (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9), a memory access priority designating unit for designating priority of memory access from the plurality of blocks (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9), a wait cycle designating unit for designating the number of wait cycles provided when memory access is requested from the plurality of blocks by the bank access data alone (Fig. 28, when an idle command is issued, by issuing the command and then issuing the next command some time later, the number of idle cycles is designated), an enabling signal generation block which is instructed by the request receiving block, **for generating** the enabling Signal and **outputting** the enabling signal to the block permitted to access the memory (Ochiai et al.: Col. 24 lines 55-67), and a control signal generation block which is instructed by the request receiving block **for generating** the control signal and **generating** each control signal (Ochiai et al.: Col. 24 lines 55-67).

5. Consider **claim 19,** as applied to **claim 15** above, Ochiai et al. discloses wherein the memory is s synchronous memory (Ochiai et al.: Col. 1 lines 20-29 and Col. 20 line 36).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. **Claims 17 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai et al. (US 6,340,973 B1).

9. Consider **claim 17,** as applied to **claim 16** above, Ochiai et al. does not explicitly state wherein the memory access priority designating unit is set from outside and priority of access from the plurality of blocks to the memory is changed according to a setting of the memory access priority designating unit, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. because, this allows for more system flexibility during various applications and also provides a better user experience.

10. Consider **claim 18,** as applied to **claim 16** above, Ochiai et al. does not explicitly state wherein the wait cycle designating unit is set from outside and the number of wait cycles provided by the command generation block is changed according to a setting of

the wait cycle designating unit, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. because, this allows for more system flexibility during various applications and also provides a better user experience.

11. **Claims 34-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai et al. (US 6,340,973 B1), and further in view of Miyawaki et al. (US 5,752,266).

12. Consider **claim 34**, Ochiai et al. discloses a memory controller for controlling a memory having a plurality of banks, **the memory controller** comprising: an arbitration circuit for arbitrating a memory access request **from a plurality of blocks** for accessing a memory (Fig. 7, Col. 24 lines 55-67 and Col. 25 lines 1-22), a command generation block for generating a memory command for a memory based on a control signal from the arbitration circuit (Fig. 1, abstract, Col. 5 lines 26-34), an address generation block **for receiving** a memory address from a block permitted **by the arbitration circuit for accessing a memory** and **outputting** the memory address to **such** memory (Fig. 1, abstract, Col. 2 lines 23-25, Col. 5 lines 20-25 and Col. 6 lines 3-7), and a data latch block **for latching either** write data from the block permitted **by the arbitration circuit for accessing a memory** or read data from a memory and **passing** data between a memory and the block (Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34), as for the limitation: wherein the arbitration circuit designates an arbitrating method for changing

priority of memory access from the plurality of blocks when the memory access request from the plurality of blocks is made to the same bank as immediately preceding access and memory access permitted by the arbitration circuit immediately before is read access (Ochiai et al. Col. 1 lines 65-67, Col. 2 lines 1-2, Col. 5 lines 1-6 and 35-40 and Col. 6 lines 45-51 and Col. 12 lines 35-38, where Ochiai et al. discloses an ordering and optimization of this ordering and reverse ordering and where ordering is performed to not have the same bank access consecutively whether the previous access was a read or not, but Ochiai et al. does not explicitly state a changing of priority of memory access, whereas Miyawaki et al. does teach this feature: abstract, Col. 1 line 67, Col. 2 lines 1-5 and Col. 4 lines 33-40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to change the priority of memory access in the system of Ochiai et al. as done in Miyawaki et al. because, Miyawaki et al. teaches that this will thereby avoid concentration on or rejection of a specific memory access operation and eliminating an ineffective period and that the user receives an efficient memory system without increasing the capacity of a buffer memory, the width of a memory bus, or an operating frequency (abstract and Col. 2 lines 3-5).

13. Consider **claim 35,** as applied to **claim 34** above, Ochiai et al. in view of Miyawaki et al. disclose wherein the arbitration circuit comprises: a bank decision unit **for receiving** a memory address from the plurality of blocks and **deciding** whether access is made to the same bank based on the received memory address (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9), an access request decision unit **for**

receiving a memory request from the plurality of blocks and **deciding** the kind of requested memory access based on the received memory request (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9, Miyawaki et al.: Col. 2 lines 1-67 and Col. 8 lines 61-67), a request receiving block which includes the bank decision unit and the access request decision unit and provides an instruction to generate an enabling signal (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9 and Miyawaki et al.: Col. 2 lines 1-67 and Col. 8 lines 61-67), a memory access priority designating unit for designating the priority of memory access from the plurality of blocks (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9), an arbitrating method designating unit for designating an arbitrating method for changing the priority of memory access when the memory access request from the plurality of blocks is made to the same bank as immediately preceding access and memory access permitted by the arbitration circuit immediately before is read access (Ochiai et al. Col. 1 lines 65-67, Col. 2 lines 1-2, Col. 5 lines 1-6 and 35-40 and Col. 6 lines 45-51 and Col. 12 lines 35-38 and Miyawaki et al.: abstract, Col. 1 line 67, Col. 2 lines 1-5 and Col. 4 lines 33-40), an identical bank priority designating unit for selecting a block to be subsequently permitted to access when the arbitrating method designating unit is set so as to place higher priority on a bank (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9), a read access priority designating unit for selecting a block to be subsequently permitted to perform read access when the arbitrating method designating unit is set so as to place higher priority on access (Miyawaki et al.: abstract, Col. 1 line 67, Col. 2 lines 1-5 and 34-67 and Col. 4 lines 33-40), an enabling signal generation block which is instructed by the

request receiving block **for generating** the enabling signal and **outputting** the enabling signal to the block permitted to access the memory (Ochiai et al.: Col. 24 lines 55-67), and a control signal generation block which is instructed by the request receiving block **for generating** the control signal and **generating** each control signal (Ochiai et al.: Col. 24 lines 55-67).

14. Consider **claim 36,** as applied to **claim 35** above, Ochiai et al. in view of Miyawaki et al. does not directly disclose wherein the memory access priority designating unit **is** set from outside and the priority of access from the plurality of blocks to the memory **is** changed according to a setting of the memory access priority designating unit, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for more system flexibility during various applications and also provides a better user experience.

15. Consider **claim 37,** as applied to **claim 35** above, Ochiai et al. in view of Miyawaki et al. does not directly disclose wherein the arbitrating method designating unit **is** set from outside and the arbitrating method of memory access from the plurality of blocks **is** changed according to a setting of the arbitrating method designating unit, however the examiner is taking official notice to the fact that a device being able to

accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for more system flexibility during various applications and also provides a better user experience.

16. Consider **claim 38,** as applied to **claim 35** above, Ochiai et al. in view of Miyawaki et al. does not directly disclose wherein the identical bank priority designating unit **is** set from outside and a block to be subsequently permitted to access to the memory **is** selected according to priority set by the identical bank priority designating unit when the arbitrating method designating unit is set so as to place higher priority on a bank and a memory access request is made from the plurality of blocks to the same bank as immediately preceding access, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for more system flexibility during various applications and also provides a better user experience.

17. Consider **claim 39,** as applied to **claim 35** above, Ochiai et al. in view of Miyawaki et al. does not directly disclose wherein the read access priority designating unit **is** set from outside and a block to be subsequently permitted to perform read access to the memory **is** selected according to priority set by the read access priority designating unit when the arbitrating method designating unit is set so as to place higher priority on access and memory access permitted by the arbitration circuit immediately before is read access, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for more system flexibility during various applications and also provides a better user experience.

18. Consider **claim 40,** as applied to **claim 34** above, Ochiai et al. in view of Miyawaki et al. disclose wherein the memory is s synchronous memory (Ochiai et al.: Col. 1 lines 20-29 and Col. 20 line 36).

19. **Claims 9, 10, 12-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai et al. (US 6,340,973 B1) in view of Miyawaki et al. (US 5,752,266) as applied to **claim 9** above, and further in view of Talbot et al. (US 6,976,135 B1).

20. Consider **claim 9**, Ochiai et al. discloses a memory controller for controlling a memory having a plurality of banks, **the memory controller** comprising: an arbitration

circuit for arbitrating a memory access request **from a plurality of blocks** for **accessing a** memory (Fig. 7, Col. 24 lines 55-67 and Col. 25 lines 1-22); a command generation block for generating a memory command for a memory based on a control signal from the arbitration circuit (Fig. 1, abstract, Col. 5 lines 26-34), an address generation block **for receiving** a memory address from a block permitted to access by the arbitration circuit and **for outputting** the memory address to the memory (Fig. 1, abstract, Col. 2 lines 23-25, Col. 5 lines 20-25 and Col. 6 lines 3-7), and a data latch block **for latching either** write data from the block permitted **by the arbitration circuit for accessing a memory** or read data from a memory and **passing** data between a memory and the block (Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34), bank access data is access data to the memory, comprising a predetermined number of bytes for performing writing or reading on the same bank of the memory, block access data is a data unit comprising two sets of the bank access data belonging to different banks, and if the plurality of blocks make a memory access request for each piece of the block access data, when a second-half bank where memory access is permitted immediately before is the same as the first-half bank of a subsequent memory access request (Col. 1 lines 31-40 and 65-67, Col. 2 lines 1-2, Col. 5 lines 1-6 and 35-40 and Col. 6 lines 45-51, Col. 7 lines 55-67, Col. 8 lines 1-55 and Col. 12 lines 35-38), where Ochiai et al. discloses an ordering and optimization of this ordering and reverse ordering, that will have consecutive requests to different banks and split-banks before consecutive requests to the same banks or split-banks, but Ochiai et al. does not

directly state that an established order **is** changed, whereas Miyawaki et al. does teach this feature: abstract, Col. 1 line 67, Col. 2 lines 1-5 and Col. 4 lines 33-40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to change the priority of memory access in the system of Ochiai et al. as done in Miyawaki et al. because, Miyawaki et al. teaches that this will thereby avoid concentration on or rejection of a specific memory access operation and eliminating an ineffective period and that the user receives an efficient memory system without increasing the capacity of a buffer memory, the width of a memory bus, or an operating frequency (abstract and Col. 2 lines 3-5).

Ochiai et al. in view of Miyawaki et al. also disclose wherein the data latch block comprises: a write data latch block which receives and latches write data from the plurality of blocks (Ochiai et al.: Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34), and a read data latch block which receives and latches the read data having been read from the memory (Ochiai et al.: Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34), as for the limitations: a data change block which, based on a data latch control signal from the arbitration circuit, changes an order of bank access data outputted by the write data latch block, outputs the data as write data to the memory, changes an order of bank access data outputted by a read data latch block, and outputs the data as read data to a block permitted to perform read access to the memory (Ochiai et al.: Col. 2 lines 33-36 and Col. 5 lines 31-35) where Ochiai et al. describes the data processor transferring and mediating the data but does not explicitly state reordering the data, whereas Talbot et al. does teach this feature (Fig. 4, abstract, Col. 5 lines 6-34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to reorder the bank access data in the data latch block in the system of Ochiai et al. in view of Miyawaki et al. because Talbot et al. teaches that doing so bandwidth **is** maximized and concurrency **is** maximized by minimizing the amount of time that memory requests must wait to be serviced (Col. 2 lines 6-31).

21. Consider **claim 10,** as applied to **claim 9** above, Ochiai et al. in view of Miyawaki et al. and Talbot et al. disclose wherein the arbitration circuit comprises: a request receiving block **for receiving** a memory request and a memory address from the plurality of blocks, **the request receiving block comprising** a bank decision unit for deciding, based on the received memory address, whether access is made to the same bank regarding a second-half bank where memory access has been permitted immediately before and a first-half bank of a subsequent memory access request, and **providing** an instruction to generate an enabling signal (Ochiai et al.: Fig. 8, Col. 7 lines 55-67, Col. 8 lines 1-23, Col. 25 lines 23-67, and Col. 26 lines 1-9), a memory access priority designating unit for designating priority of memory access from the plurality of blocks (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9), an enabling signal generation block which is instructed by the request receiving block **for generating** the enabling signal and **outputting** the enabling signal to the block permitted to access the memory (Ochiai et al.: Col. 24 lines 55-67), and a control signal generation block which is instructed by the request receiving block **for generating** the control signal (Ochiai et al.: Col. 24 lines 55-67).

22. Consider **claim 12,** as applied to **claim 9** above, Ochiai et al. in view of Miyawaki et al. discloses all the limitations of **claim 9** above, but as for the limitation: wherein when the second-half bank where memory access has been permitted immediately before is the same as the first-half bank of the subsequent memory access request, the arbitration circuit changes an order of the bank access data in the block access data, reads the block access data from the memory, and stores the data in the data latch block, and the data latch block changes an order of each piece of the bank access data in the block access data and transfers the data to the block having performed memory access(Ochiai et al.: Col. 2 lines 33-36, Col. 5 lines 31-35, Col. 7 lines 55-67, and Col. 8 lines 1-23) where Ochiai et al. describes the data processor transferring and mediating the data but does not explicitly state reordering the data, whereas Talbot et al. does teach this feature (Fig. 4, abstract, Col. 5 lines 6-34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to reorder the bank access data in the data latch block in the system of Ochiai et al. in view of Miyawaki et al. because Talbot et al. teaches that doing so bandwidth **is** maximized and concurrency **is** maximized by minimizing the amount of time that memory requests must wait to be serviced (Col. 2 lines 6-31).

23. Consider **claim 13,** as applied to **claim 10** above, Ochiai et al. in view of Miyawaki et al. do not explicitly state wherein the memory access priority designating unit is set from outside and the priority of access from the plurality of blocks to the memory is changed according to a setting of the memory access priority designating unit, however the examiner is taking official notice to the fact that a device being able to

accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for more system flexibility during various applications and also provides a better user experience.

24. Consider **claim 14,** as applied to **claim 9** above, Ochiai et al. in view of Miyawaki et al. disclose wherein the memory is s synchronous memory (Ochiai et al.: Col. 1 lines 20-29 and Col. 20 line 36).

Response to Arguments

25. Applicant's arguments filed 12/21/2007 have been fully considered but they are not persuasive.

26. Applicant argues, with respect to **claims 15, 16 and 19**, the limitation "the arbitration circuit instructing the command generation block to provide a wait cycle when a memory access request is made by the bank access data alone from the block permitted to access the memory", more specifically that the idle state of the SDRAM is not a wait cycle as claimed, however Ochiai et al. teaches in fig. 28 and col. 1 lines 41-64 that when a request is made to a column of a page of a bank, the column of the page in the bank is precharged and then an idle(wait) state occurs before the column, page and bank combination are accessed, therefore meeting the claim limitation. The applicant also emphasizes the term "alone" within the limitation "when a memory access

request is made by the bank access data alone from the block permitted to access the memory" stating that Ochiai is simply silent regarding this feature, however Applicant's argument merely amounts to a general allegation that the claim limitation defines a novel feature without specifically pointing out how the language is patentably distinct from the Ochiai reference, the applicant has not addressed or described how the claim limitation is not met by the cited portions of Ochiai reference by the examiner. Applicant also argues that Ochiai fails to disclose the limitation "block access data…comprising two sets of the bank access data belonging to different banks", specifically that the data block in Ochiai fails to describe the block access data, however Ochiai et al. discloses that sets of bank accesses are ordered and grouped so that consecutive requests are to different banks and split-banks before accesses to the same bank or split-bank, therefore disclosing grouping bank access data so that they are to different banks, therefore meeting the claim limitation. This same rational applies to the argument in **claim 9** about the block access data.

27. Also, with respect to **claim 9**, applicant argues that Ochiai in view of Miyawaki does not disclose the limitation "when a second-half bank where memory access is permitted immediately before is the same as the first-half bank of a subsequent memory access request, the arbitration circuit changes an order of memory access of the bank access data in the block access data,", more specifically that the ordering is not performed: "when a second-half bank where memory access is permitted immediately before is the same as the first-half bank of a subsequent memory access request,", however Ochiai describes ordering memory accesses so that consecutive accesses are

to different banks, Miyawaki discloses changing the ordering of the memory accesses depending on the situation in the memory, this combination therefore discloses reordering the memory access to have consecutive access to different memory banks, if they are not present in that format. The examiner would also like to note that even though Ochiai does not directly state the term reordering, however memory accesses are generated based on the need of the processor then ordered into the desired format, therefore being a reordering as well.

Conclusion

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-

1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Michael Alsip
Examiner
Art Unit 2186

/Michael Alsip/
Examiner, Art Unit 2186

March 5, 2008